

8D Report for ALT STB BFX-UA300 Choke Burned and FFC Cable Melted Issue

Date : 2022-March-26
Version: 01

D1. Establish the Team

FII Team

- **Team Leader**

RD: Rick Chen

QA: CB Lin

- **Team Member**

RD: Sean Jiang

PE: Jack Han, Michael

QA: Toney, Rachel

TE: Mark

PM: Ben

VGT Team

QA: Jacob Chen, Yang Hua

CQE: Kevin Wu

PD: Xiao Sha

ME: Wu yong

D2. Description of Problems

- On 2021-Feb-04, ALT customer feedback that 1pcs BFX-UA300 field defect.
- Defect Symptom:** FFC cable melted, and T1 component (choke) burned.
- Defect Rate:** 1/4,796 = 0.02% [D/C 2136 Q'ty 4,796pcs]
- S/N:** 2149695001202109001829



FFC cable melted



T1 component (choke) burned

Part	P/N	Vendor	D/C	L/C
FFC cable	376.00039.005	P-TWO	202140	-
Choke (T1)	155.00089.005	CHILISIN	2135	V96-152400006HZ
PCB	308.03581.055	VG T	2136	202109-0001

D3. Containment Actions

1. FII Containment Action

No WIP & stock products with PCB D/C 2136 at FII.

PQE: Rachel, Done on Feb-05

2. VGT Containment Action

No WIP, no on the way PCB.

154pcs (D/C 2151) at stock, 100% retest E-test, all of them test PASS.

VGT PD: Xiao Sha, Done on Mar-01

D4. Root Cause Analysis – Factory Production Data Check

1. Factory production data check

1.1 Check the SFIS records of this defect product, no test fail record. ➔ No repair, no abnormal found.

This product shipped on 08-Nov-2021, it belong to the first lot 300 units.

SERIAL_NUMBER	SHIPPING_SN	GROUP_NAME	IN_STATION_TIME	ATE_STATION_NO
A8934AFE7F19	N/A	ASSY	11/5/2021 2:43:49 AM	
A8934AFE7F19	N/A	BT	11/5/2021 4:18:44 AM	L09K18BT0001
A8934AFE7F19	N/A	PT	11/5/2021 4:23:30 AM	L09K18PT0002
A8934AFE7F19	N/A	UP	11/5/2021 4:25:37 AM	L09K18UP0001
A8934AFE7F19	N/A	ASSY2	11/6/2021 7:34:07 PM	
A8934AFE7F19	N/A	ASSY3	11/6/2021 7:43:26 PM	
A8934AFE7F19	N/A	ASSY4	11/6/2021 7:50:20 PM	
A8934AFE7F19	N/A	FT1	11/6/2021 7:59:39 PM	L09K18FT1001
A8934AFE7F19	N/A	FT2	11/6/2021 8:05:35 PM	L09K18FT2001
A8934AFE7F19	N/A	FT3	11/6/2021 8:10:03 PM	L09K18FT3001
A8934AFE7F19	N/A	RC	11/6/2021 8:12:17 PM	L10K18RC0001
A8934AFE7F19	N/A	RC1	11/6/2021 8:18:58 PM	L09K18RC1001
A8934AFE7F19	N/A	VI	11/7/2021 3:56:31 AM	
A8934AFE7F19	2149695001202109001829	RC2	11/7/2021 3:58:43 AM	L09K18RC2001
A8934AFE7F19	2149695001202109001829	VI1	11/7/2021 4:06:19 AM	
A8934AFE7F19	2149695001202109001829	PACK_BOX	11/7/2021 4:20:10 AM	
A8934AFE7F19	2149695001202109001829	CHECK_WEIGHT	11/7/2021 4:28:12 AM	
A8934AFE7F19	2149695001202109001829	PACK_CTN	11/7/2021 4:28:40 AM	
A8934AFE7F19	2149695001202109001829	PACK_PALT	11/7/2021 7:41:50 AM	
A8934AFE7F19	2149695001202109001829	FQA	11/7/2021 7:56:43 AM	
A8934AFE7F19	2149695001202109001829	STOCKIN	11/7/2021 8:34:39 PM	

D4. Root Cause Analysis – Factory Production Data Check

1. Factory production data check

1.2 Check the test log files of all test stations, the test logs are normal, the functions test PASS.

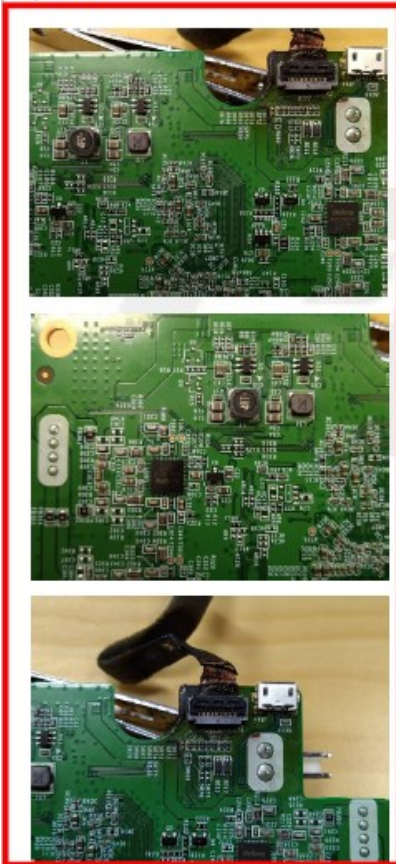
MAC ID	Shipping SN	Test Log					
A8934AFE7F19	2149695001202109001829	 FT1_PASS_A8934 AFE7F19_.doc	 FT2_PASS_A8934 AFE7F19.doc	 FT3_PASS_A8934 AFE7F19.doc	 RC_PASS_A8934 AFE7F19.doc	 RC1_PASS_A8934 AFE7F19.doc	 RC2_PASS_A8934 AFE7F19.doc

D4. Root Cause Analysis – FII RD FA @VI Inspection

2. FII RD FA

2.1 VI inspection: Take apart of AMP board.

Top side



Bottom side



- At top side:
 1. 24V trace had charred and FFC connector was burned out.
 2. The other circuits look ok and are not affected.
- At bottom side:
 1. SOC, eMMC, and other circuit are ok.
 2. 24V power choke and capacitors were burned out at 24V frond end.

D4. Root Cause Analysis – FII RD FA @VI Inspection

2. FII RD FA

2.1 VI inspection: Take apart of AMP board.

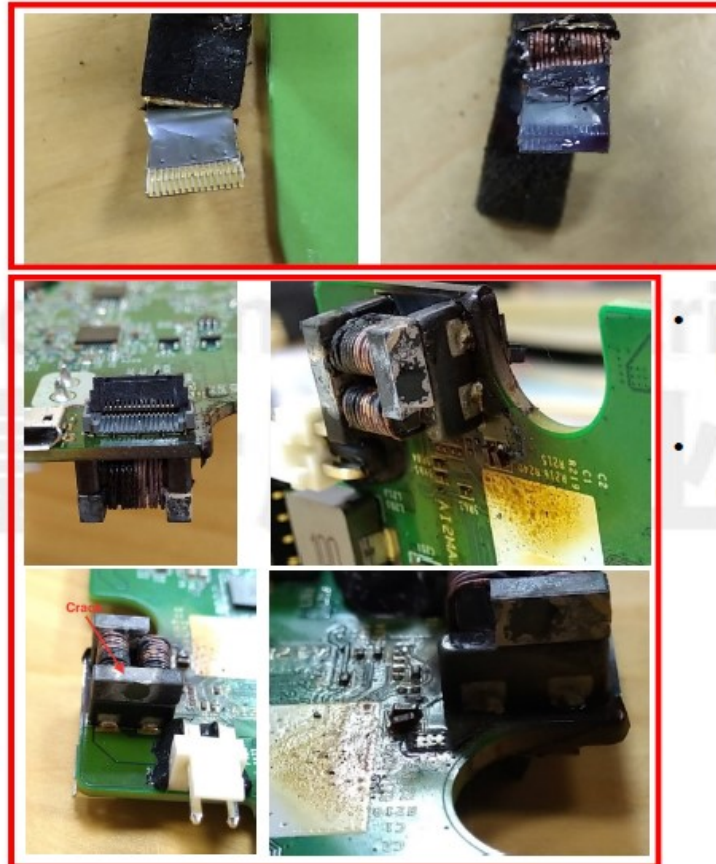
FA step:

1. VI inspection

Other detail pictures.



- Top side of FFC cable and foam seriously burned out.
- FFC cable trace is exposed.



- FFC cable:
Bottom: golden fingers are ok.
Top: Burned out mark.

- 24V trace of PCB is going to peel off by burned out.
- The core of choke has crack and damaged.

D4. Root Cause Analysis – FII RD FA @Circuit Analysis

2. FII RD FA

2.2 Measure the impedance of power trace.

- Only 24V circuit is short to GND.

Unit: Ohm			VDD_EE	1.35V	VDDCPU	3.3V
	24V	5V	L52	L53	L51	L2
Defect AMP board	3.3	43.3K	454	1.72K	573	14.66K
OK AMP board	35.05K	43.3K	454	1.79K	659	15.39K

2.3 Cut off 24V trace to isolate power choke circuit.

- After cutting off 24V power trace, the short is in choke circuit.

Unit: Ohm	Bottom	Top	Choke circuit
Defect AMP board	5.27M	6.5M	0.3

2.4 Remove components

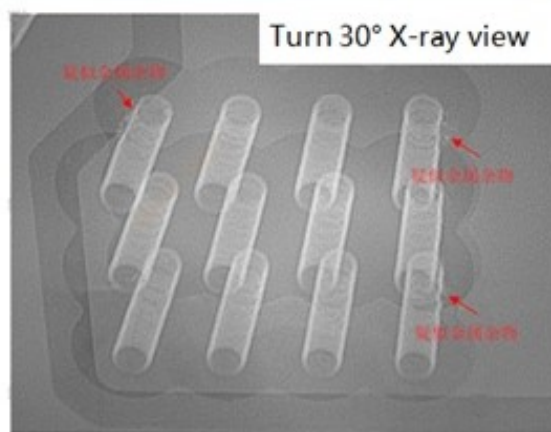
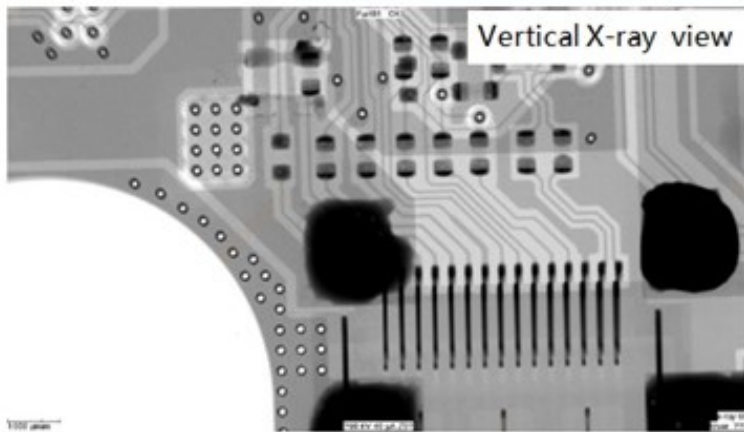
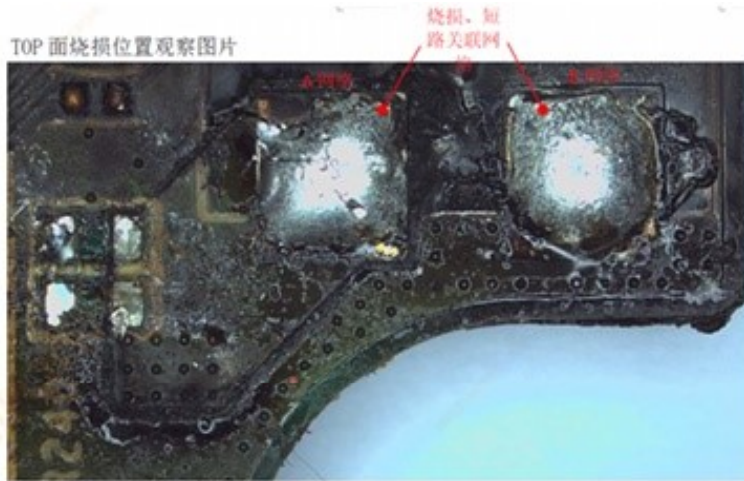
- Remove components as choke and C1/C2 capacitor, PCB is still short to GND.
- Suspect PCB power trace on 24V at choke circuit is short to GND.

PCB vendor: VGT

D4. Root Cause Analysis – VGT FA @X-Ray Inspection

3. VGT FA

3.1 X-Ray inspection – see some material around the through holes.



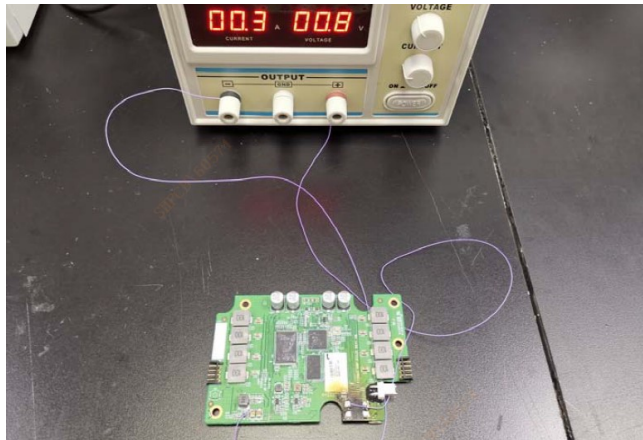
X-ray check, see some material around the through holes.

D4. Root Cause Analysis – VGT FA @Thermal Imaging Check

3. VGT FA

3.2 Thermal imaging check – the short location should be in the through hole.

1) energized 0.3A current to A/B circuit , to make the short point hot.



2) Thermal imaging device to view the top side : the hot location is in the through hole area.



3) Thermal imaging device to view the bottom side : the hot location is still in the through hole area.



D4. Root Cause Analysis – VGT FA @Micro-section Observe

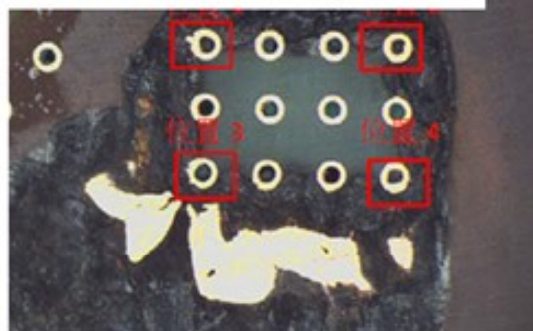
3. VGT FA

3.3 Make horizontal micro-section observe – the short location in the PCB layer 2.

1) Grind off the Top side(L1), the short still exists.



2.1) Observe L2 layer, some melted copper is found around the through hole.



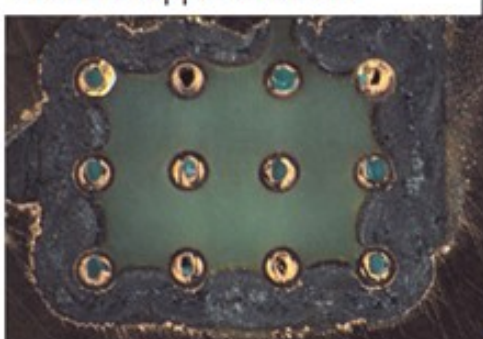
2.2) L2 layer design:



3) Grind off the bottom side(L4 layer), test the A,B network, the short still exists:



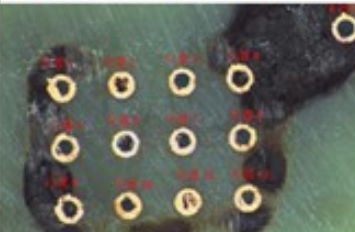
4.1) Observe the L3 layer, no residual copper is found.



4.2) L3 layer design:



5) Grind off the L3 layer, but leave the L2 layer, test the through holes, which connects A and B network, there still has value of resistance.



位置1	位置2	位置3	位置4
8.426KΩ	411.05Ω	187.19Ω	1.0945KΩ
位置5	位置6	位置7	位置8
61.49KΩ	29.441MΩ	67.4MΩ	0.932KΩ
位置9	位置10	位置11	位置12
4.1661KΩ	17.892KΩ	0.504KΩ	1.8188KΩ

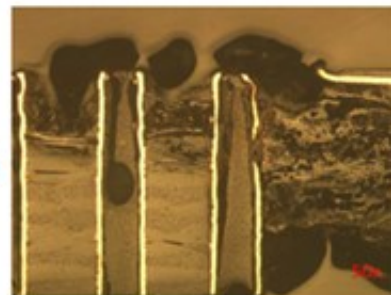
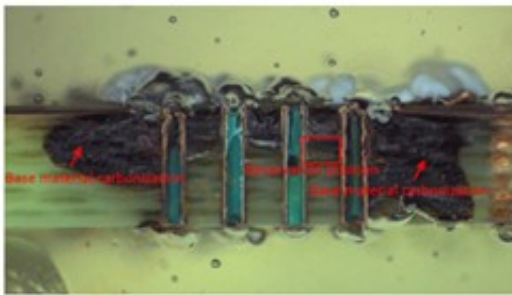
Summary : confirmed that the short point exists in the layer 2

D4. Root Cause Analysis – VGT FA @SEM observation

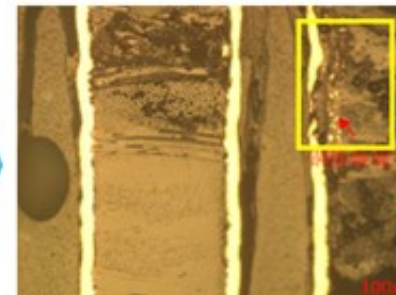
3. VGT FA

3.4 SEM observation – the lamination is cracked and melted copper could be found in the crack of the lamination.

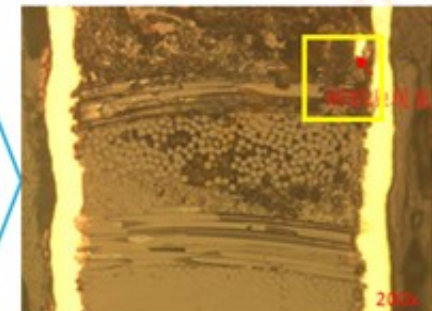
SEM observation:



50X



100X, melted copper could be found c.



200X, melted copper could be found in the lamination



SEM observation summary:
500X, the lamination is cracked and melted copper could be found in the crack of the lamination



500x

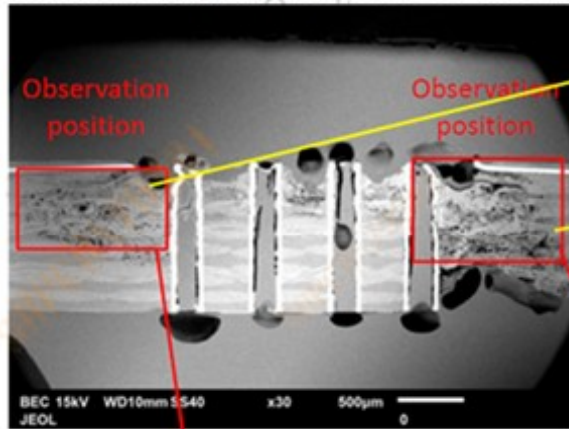
D4. Root Cause Analysis – VGT FA @SEM observation

3. VGT FA

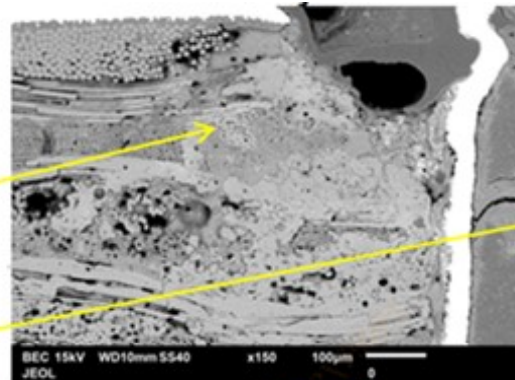
3.4 SEM observation – the lamination is cracked and melted copper could be found in the crack of the lamination.

SEM observation:

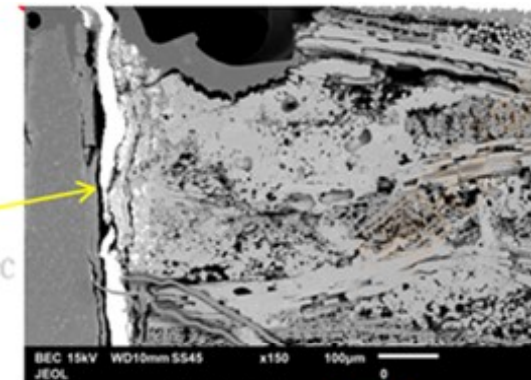
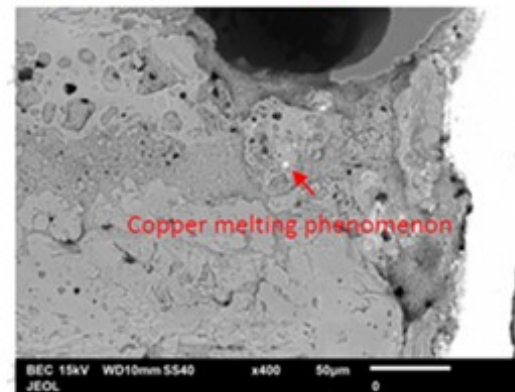
Schematic diagram of section observation



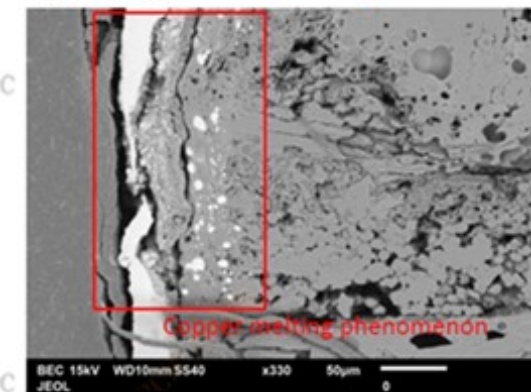
SEM observation summary:
the lamination is cracked and
melted copper could be
found in the crack of the
lamination.



magnification



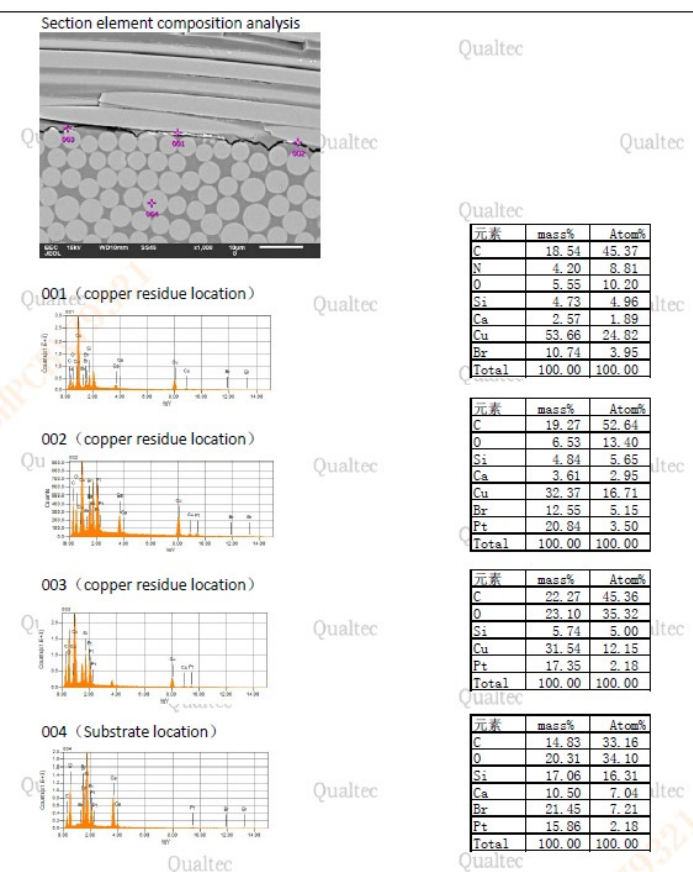
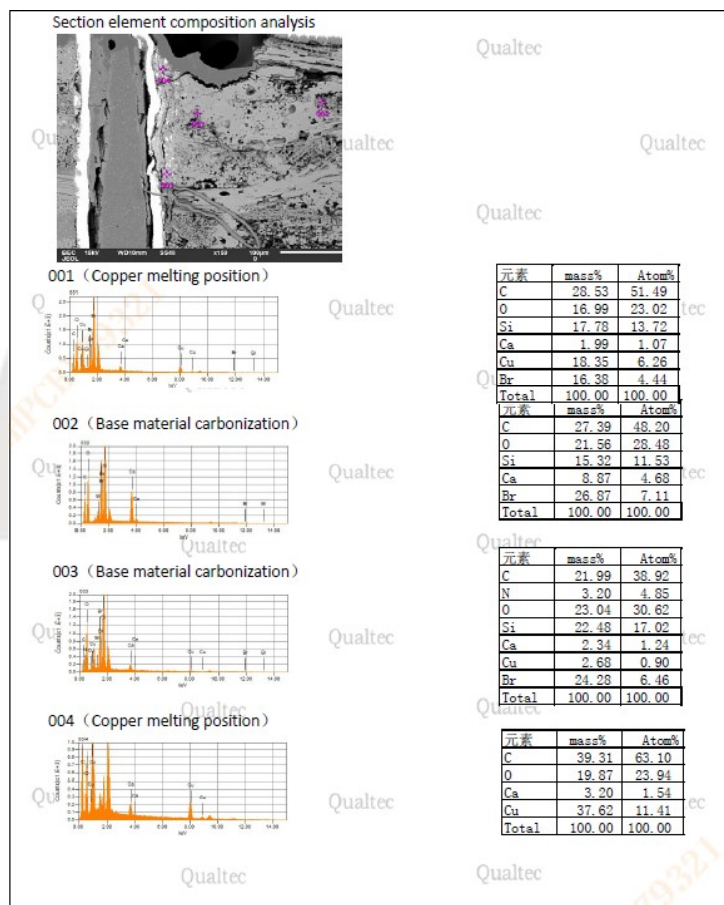
magnification



D4. Root Cause Analysis – VGT FA @EDX Analysis

3. VGT FA

3.5 EDX analysis – Confirmed the material in the crack of lamination is melted copper.



D4. Root Cause Analysis – VGT FA Summary

3. VGT FA

3.6 VGT FA summary

After above analysis to the returned PCBA, summarize the FA result as below:

- Thermal imaging check showed that the short location should be in the through hole.
- Made horizontal micro-section observe confirmed that the short circuit happen in layer2.
- By SEM, some melted copper could be found around the 4 through holes and in the crack of lamination. Also, the lamination grew some cracks due to the burning or some other forces such like hot air swelling.
- EDX analysis to confirm the material in the crack of lamination is melted copper.

D4. Analysis Root Cause – FII/VGT FA Summary

4. Summary for FII / VGT FA

➤ FII FA result:

- Suspect PCB power trace on 24V at choke circuit is short to GND.

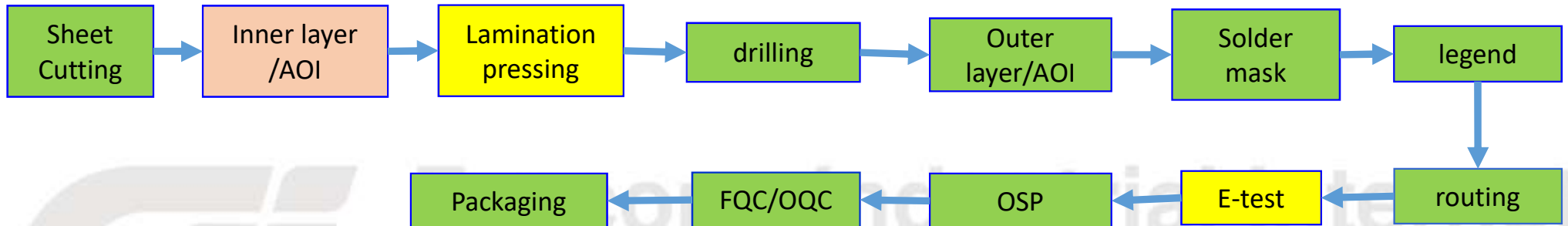
➤ VGT FA result:

- Short circuit happen in layer2, around the through holes.
- By SEM, some melted copper could be found around the 4 through holes and in the crack of lamination.
- EDX analysis to confirm the material in the crack of lamination is copper.

D4. Root Cause Analysis – VGT PCB Process Analysis

5. VGT PCB production process analysis.

5.1 PCB Overall Flow Chart.



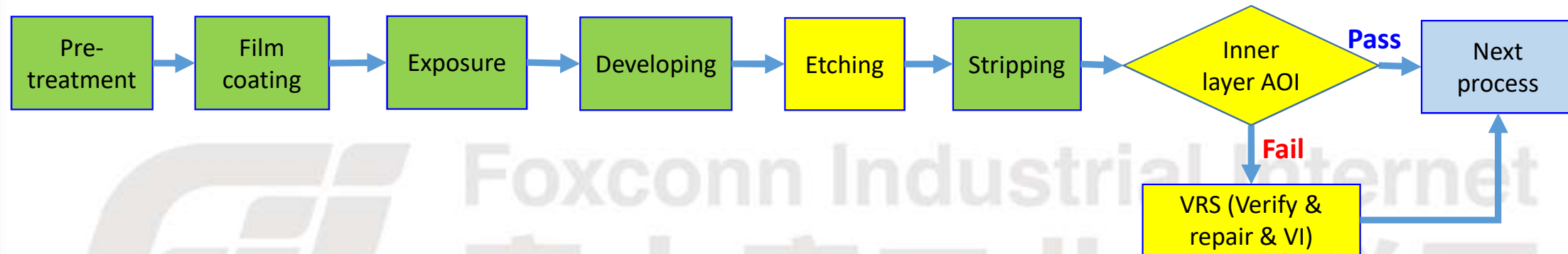
From the overall PCB production flow, the possible stations for L2 inner layer short is:

- **Inner layer process** [refer to next page]
- **Lamination pressing station** [Occur] - Residual copper may happen in the Lamination pressing process.
- **E-test station** [Escape] - It can cover the open/short defect.

D4. Root Cause Analysis – VGT PCB Process Analysis

5. VGT PCB production process analysis.

5.2 L2 Inner layer flow chart



From the L2 inner layer flow, the possible stations for L2 inner layer short is:

- **Etching station** [Occur] - Residual copper in the inner layer may happen in the etching process.
- **Inner layer AOI station** [Escape] - AOI can cover the short defect, but it maybe bypass by AOI operator.
- **VRS station** [Escape] - Only visual inspection the repaired PCB, it's better to retest AOI.

D4. Root Cause Analysis – VGT PCB AOI/E-test Yield Rate

5. VGT PCB production process analysis.

5.3 PCB production records.

☐ Inner layer AOI – Target: 97.5%

- Total produced 256 panels on 2021-Aug-26.
- L2 pass rate 99.09%, met the AOI target; Short*2pcs @defect rate 0.13%.

☐ E-Test

- E-test parameter: Insulation voltage: 250V, Conduction value: $\leq 50\Omega$, Insulation value: 10Mohm
- E-test detected 14pcs short defect, and 1pc short at L2 layer, the defect rate was 0.02%.

Part number	DC	E-test quantity	Short quantity	layer	quantity	Failure rate	Pass rate	result	Defect description	FM
308.03524.055	2136	4180 pcs	14 pcs	L1	5	0.2%	94%	pass	Metal fragment Of inner layer	
				L2	1	0.02%	94%	pass		
				L3	2	0.047%	94%	pass		
				L4	6	0.014%	94%	pass		

D4. Analysis Root Cause – Root Cause Summary

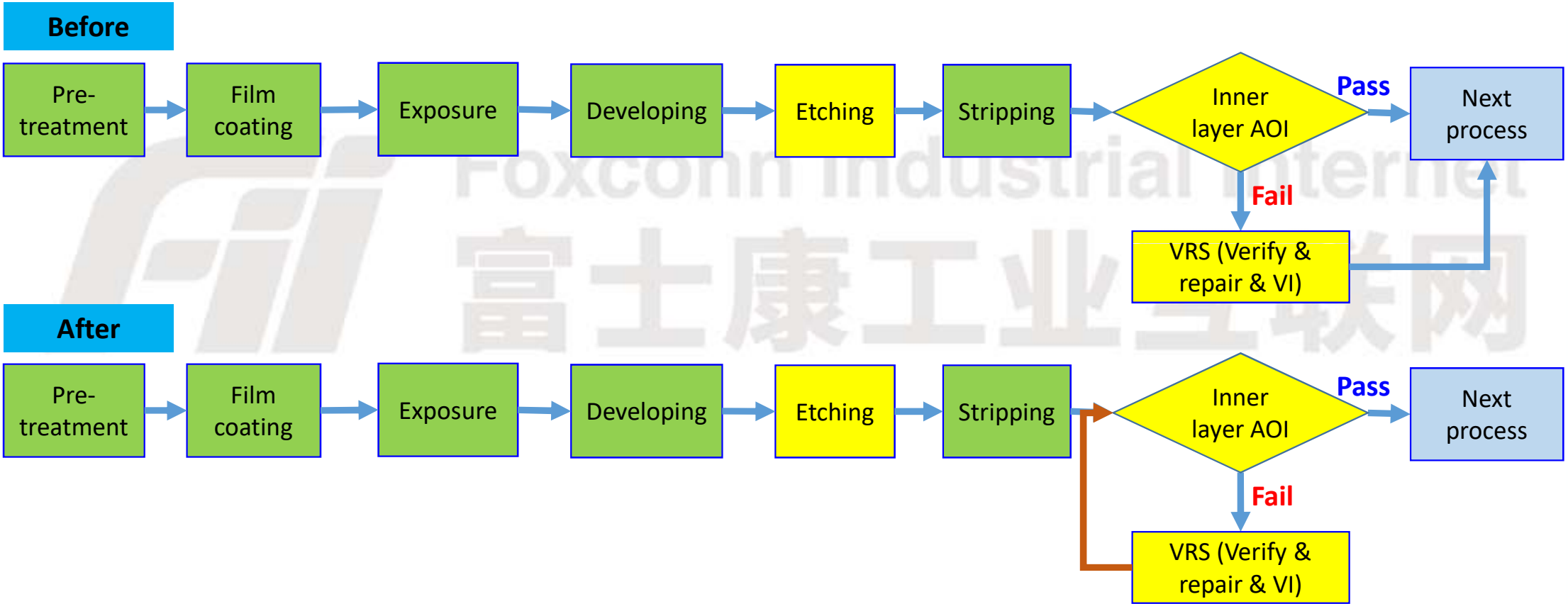
6. Summary for root cause analysis

- **VGT PCB L2 layer short - residual copper [Possible Occur Reason]**
 - PCB Layer 2 **Etching process** maybe cause residual copper.
 - PCB **Lamination pressing process** maybe cause residual copper.
 - **VRS station** after AOI - Only visual inspection the repaired PCB.
- **VGT PCB L2 layer short - residual copper [Possible Escape Reason]**
 - PCB Layer 2 **Inner layer AOI station** can cover the short defect, but it maybe bypass by AOI operator.
 - **E-test station** can cover the open/short defect.

D5. Corrective Actions

1. Optimize the VRS process, repaired PCB must 100% AOI. Implement D/C 2212.

Owner: VGT/Kevin, Done on Mar-25



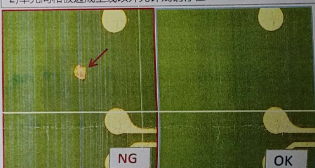
D5. Corrective Actions

2. VGT enhance the AOI inspector training, and hang the defect picture at the AOI station.

Owner: VGT/Kevin, Done on Mar-21

胜宏科技（惠州）股份有限公司
VICTORY GIANT TECHNOLOGY (HUIZHOU) CO., LTD.

内检教育培训 (OPL)

主题	S47304PNM39D2烧板客诉教育培训					
分类	☐ 基础知识 ☐ 改善事项 ☐ 故障 ☒ 品质 ☐ 安全 ☐ 事例 ☐ 其它 _____					
目的	使员工了解功能性客诉的项目，在后续检验过程中进行卡关。					
作业要点	1、课长召集白/晚班检验员进行检讨。 2、每日开班前小组会议时组长对客诉内容进行宣导，严防品质漏失。 3、后续扫描出来的残铜100%需按要求处理。 4、修理后的板需100%重新扫描检测。					
作业图片	S47304PNM39D2客诉烧板不良，经分析烧板位置存在内层残铜 检修岗位应按以下标准严格执行： 1) 成型线以内任何区域不允许有残铜； 2) 单元间和板边成型线以外允许残铜存在  					
讲师	何勇	日期	2022.3.21	应到人数	10	
实到人数	10	签名: 陈 彭平 杨 余辉 刘文强 袁亚明 魏鹏 (苏以民 吴晓林 田飞鸣)				
制作	段周宁	审核	何勇			

D6. Verification the Corrective Actions

VGT will monitor the effectiveness at the following 3 months.

Owner: VGT/Kevin, Due date: Jun-30



Foxconn Industrial Internet
富士康工业互联网

D7. Preventive Actions

Document the optimized VRS process - repaired PCB must 100% AOI.

Owner: VGT/Kevin, Done on Mar-25

厂内料号: S47304PNM39A1
客户料号: 308.03581.045
终端料号:
制造分厂: 胜宏六处 层别: L1-L4 第 1 页, 共 3 页

胜宏科技 (惠州) 股份有限公司
VICTORY ELECTRONIC TECHNOLOGY (HUIZHOU) CO., LTD.
制作流程单

序号: 1
层数: 4



流程单号	订单数量	投料数量	PCS	批号:	订单状态:
下料日期	生管交期	生产数量	片	本批PCS数:	
过账站别	制程名称	注意事项	移出数量	报废数量	建档人员/机台
					IPQC 签收盖章
					转出时间 日期 时间
开料	裁板/圆角	锯板损耗4mm 基板批号:			
	圆角				
	磨边				
内层	内层前处理涂布	1.底片类型:负			
	内层曝光	1.原稿线宽:4 mil 2.工作稿线宽:4.91 mil 3.线宽管控层别:L3 4.原稿间距:4 mil 5.工作稿间距:3 mil 6.间距管控层别:L3 孔距铜min: 8 mil.孔距线min: 6 mil			
	内层DES&AOI	1.成品线宽:3.91 mil 2.线宽管控层别:L3 3.成品间距:4 mil 4.间距管控层别:L3 线宽≤5mil时按±1mil管制,线宽≥5mil时按±20%管制,阻抗线宽公差见阻抗信息表 内层转LDI机台代工作业!			
内层AOI	内层VRS&修补	过AOI检查			
	内层修补				
压合	PE/冲孔&棕化				
	PP裁切	PP批号:			
	预叠	:			
	压合	介层厚度(基板及PP)公差:±10%			
		PP批号:			
		铜箔批号:			
		:			

100% AOI after repair PCB

D8. Congratulation Your Team



Thank you!

Foxconn Industrial Internet
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